UNITED STATES DEPARTMENT OF COMMERCE
Patent and Trademark Office
Address: COMMISSIONER OF PATENTS AND TRADEMARKS
Washington, D.C. 20231

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.
09/170,625	10/13/98	CHOI	D 8733D-6836

MMC2/0202

LOEB & LOEB
10100 SANTA MONICA BLVD SUITE 2200
LOS ANGELES CA 90067-4164

EXAMINER	
HAWRANEK, S	
ART UNIT	**PAPER NUMBER**
2823	

DATE MAILED: 02/02/01

Please find below and/or attached an Office communication concerning this application or proceeding.

Commissioner of Patents and Trademarks

Office Action Summary	Application No. 09/170,625	Applicant(s) CHOI, DUCK-KYUN	
	Examiner Scott J Hawranek	Art Unit 2823	

-- Th MAILING DATE of this communication appears on th cov r sheet with the correspond nce address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136 (a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *22 November 2000* .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-36* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *1-36* is/are allowed.

6)☐ Claim(s) _____ is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claims _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are objected to by the Examiner.

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. § 119

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. § 119(e).

Attachment(s)

15) ☐ Notice of References Cited (PTO-892)
16) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
17) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
18) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
19) ☐ Notice of Informal Patent Application (PTO-152)
20) ☐ Other: .

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-36 are rejected under 35 U.S.C. 103(a) as being unpatentable over the combination of Maekawa (US Pat No. 6,066,547), Arai et al. (US Pat No. 5,576,222) and Seung-Ik Jun (Aepse '97) and/or Cristoloveanu et al. (SOI).

Maekawa discloses in figures 1-20 and related text forming a TFT forming an amorphous silicon layer as an active layer on a glass substrate or quartz (fig. 8, 14) with an oxide; forming a gate insulating layer (fig. 8, 18) and a gate electrode on the amorphous silicon layer (fig. 8, 20); doping impurities of a first conductive type in the amorphous silicon layer (fig. 8, 22); forming a metal layer of less than 30A (col. 6) on the exposed portions of the amorphous silicon layer (fig. 8, 24); and crystallizing the amorphous silicon layer by applying thermal treatment. With the formation of at least the first electrode prior to the recrystallization step; source/drain regions formed prior to the crystallization step. It is held, absent evidence to the contrary, that the subsequent use of the TFT would require the formation of source/drain contracts in which an electric field on the substrate would be generated via the current. See In re Best, 195 USPQ 428 (CCPA 1977) and In re Fitzgerald, 205 USPQ 594 (CCPA 1980).

Examiner official notice of the selection of PH3 as a dopant was not seasonably contested as such is taken as admitted prior art.

Maekawa teaches forming the gate electrode from a semiconductor film (20) selected from a group consisting of polycrystalline silicon, refractory metals, and other conventional semiconductor materials that are suitable. (col. 5, line 60-65)

Arai et al. (US Pat No. 5,576,222) discloses in figs. 1-7(B) forming an conventional gate electrodes from doped amorphous silicon layer (fig. 2(f), 5') and forming an active layer of amorphous silicon (fig. 2(f), 3') then converting both layers simultaneously into polycrystalline layers which is a conventional semiconductor material. Therefore, it would have been obvious to one of ordinary skill in the art to combine the teachings of Arai et al. with Maekawa for the disclosed intended purpose of forming a gate electrode.

Arai et al. and Maekawa lack anticipation for annealing the amorphous silicon layer into polycrystalline utilizing an electric field to the resultant substrate.

Seung-Ik Jun (Aepse '97) discloses utilizing field aided lateral crystallization (FALC) utilizing a thin layer of nickel as a catalyst (~30A) at around 500 [C] on and amorphous silicon in order to obtain a high quality film of polycrystalline and other disclosed reasons. It would have been obvious to one of ordinary skill in the art to utilized the FALC in order to obtain a high quality film and combine Jun's teachings with Arai and Maeakawa.

Cristoloveanu et al. (SOI) discloses in figs. 1-6 and related discloses utilizing FALC in order to achieve polycrystalline silicon from amorphous silicon it would have been obvious to

one of ordinary skill in the art to combine the teachings with Critoloveanu with Arai and Maekawa in order to achieve polycrystalline films.

Response to Arguments

2. Applicant asserts, "Seung-Ik Jun presents only a proposed fabrication technology for producing thin film transistors by crystallizing an amorphous silicon layer using heat and electric fields. Seung-Ik Jun does not state that the proposed fabrication works." However, it appears applicant does admit that Seung-Ik Jun does disclose utilizing field aided lateral crystallization (FALC) utilizing a thin layer of nickel as a catalyst (~30A) at around 500 [C] on and amorphous silicon. One of ordinary skill in the art at the time of the invention would have been able to take the teachings of Seung-Ik Jun and perform the disclosed process, therefore, applicant's arguments are not persuasive.

Applicant asserts, "Cristoloveanu et al. simply teach using heat and electric field to convert amorphous silicon into polysilicon. Significantly, there is no discussion of using their method to fabricate thin-film transistors by converting amorphous silicon into poly-silicon using heat and electric fields. Even more significantly, there is no teaching that their technique would enable the production of produce thin-film transistors." However, the rejection is not overcome by pointing out that one reference does not contain a particular teaching when the relevance for that teaching was on the other reference. In Re Lyons 150 PQ41. Unobviousness cannot be established by attacking references individually when rejection is based on combination of references. Ex Parte Campkell 172 USPQ 91, In Re Young 159 USPQ 725.

It is established that the selection of PH3 as a dopant is notoriously obvious in the art because applicant has not seasonably contested the assertion made in the statement of the rejection of claims under 35 USC 103 in the office action mailed 11/22/00. See MPEP 2144.03.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Scott J. Hawranek whose telephone number is (703) 305-0070. The examiner can normally be reached on Monday thru Friday from 8:30 to 6:00 P.M. .

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wael M. Fahmy, can be reached on (703) 308-4918. The fax phone number for this Group is (703) 308-7722.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Group receptionist whose telephone number is (703) 308-1778.

Scott J. Hawranek
Art Unit: 2823
February 1, 2001

Charles Bowers
Supervisory Patent Examiner
Technology Center 2800